LISTING OF CLAIMS:

1. (Original) A tiered power regulation system comprising:

a first power regulator; and

an array comprising a plurality of second power regulators, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands,

wherein said array comprising a plurality of second power regulators is configured to couple to a plurality of portions of a microprocessor.

2. (Original) The tiered power regulation system of claim 1, wherein said regulator array is coupled to said microprocessor using bump technology.

3. (Original) The tiered power regulation system of claim 1, wherein said regulator array is formed using a compound semiconductor substrate.

4. (Original) The tiered power regulation system of claim 1, wherein said first regulator is a switching regulator.

5. (Original) The tiered power regulation system of claim 1, wherein said second power regulators are coupled together in parallel.

6. (Original) The tiered power regulation system of claim 1, wherein said first regulator provides power to said array and to said microprocessor.

7. (Original) The tiered power regulation system of claim 1, further comprising electronic components coupled to said microprocessor, said components configured to provide power to said microprocessor.

8. (Original) The tiered power regulation system of claim 1, wherein said array is coupled in parallel to said first regulator and to said microprocessor.

9. (Original) A tiered power regulation system comprising:

a first power regulator;

a microelectronic device formed on a first substrate; and

an array of second power regulators formed on a second substrate, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands.

10. (Original) The tiered power regulation system of claim 9, wherein said microelectronic device and said array are coupled together using bump technology.

11. (Original) The tiered power regulation system of claim 9, wherein the first power regulator is a Buck regulator.

12. (Original) The tiered power regulation system of claim 9, wherein the microelectronic device comprises a microprocessor.

13. (Original) The tiered power regulation system of claim 9, wherein the second substrate comprises compound semiconductor material.

14. (Original) The tiered power regulation system of claim 9, wherein said second power regulators are coupled together in parallel.

15. (Original) The tiered power regulation system of claim 9, wherein said first regulator provides power to said array and to said microelectronic device.

16. (Original) The tiered power regulation system of claim 9, further comprising electronic components coupled to said microelectronic device, said components configured to provide power to said microelectronic device.

17. (Original) The tiered power regulation system of claim 9, wherein said array is coupled in parallel to said first regulator and to said microelectronic device.

18. (Original) A tiered power regulation system comprising:

a first power regulator;

a microelectronic device formed on a first substrate; and

an array of second power regulators formed on a second substrate, said second power regulators configured to respond to a load power demand rate greater than said first power regulator responds to power demands,

wherein said array is coupled in parallel to said microelectronic device using bump technology.